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09/580,854	05/30/2000	Supamas Sirichotiyakul	SC91051A	1516

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Motorola Inc
Austin Intellectual Property Law Section
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EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	4

DATE MAILED: 10/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/580,854	SIRICHOTIYAKUL ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-20,32-38,41,42 and 44* is/are allowed.

6)☒ Claim(s) *21-29,31,39,40 and 43* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-44 of the application have been examined.

Drawings

2. The drawings submitted on 30 May 2000 are accepted.

Specification

3. The disclosure is objected to because of the following informalities:

Page 1, Line 11, "through the use of lower supplier voltages" appears to be incorrect and appears that it should be "through the use of lower supply voltages".

Page 12, Lines 11, "partitions into which the circuit can divided" appears to be incorrect and appears that it should be "partitions into which the circuit can be divided".

Appropriate corrections are required.

Claim Objections

4. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

5. Claim 42 is objected to because of the following informalities:

Claim 42, Lines 1-2, "calculating a leakage current for the at leas tone DCC corresponding to the dominant logic state" appears to be incorrect and appears that it should be "calculating a leakage current for the at least one DCC corresponding to the dominant logic state".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 39 and 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 39 recites the limitation " The method of claim 30, wherein the first set of transistors and the second set of transistors are mutually exclusive ". There is insufficient antecedent basis for this limitation in claim 30.

Claim 40 recites the limitation " The method of claim 30, further comprising calculating a leakage current of the integrated circuit by summing the leakages for the transistors in the first set and the leakages for the transistors in the second set". There is insufficient antecedent basis for this limitation in claim 30.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 21, 25, 27-29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Reyes et al. (RE)** (U.S. Patent 5,774,367) in view of **Pullela et al. (PU)** U.S. Patent 5,751,593).

10.1 **RE** teaches method for selecting device threshold voltages for high speed and low power. Specifically, as per Claim 21, **RE** teaches a method of improving performance of an integrated circuit (Fig. 2; CL2, L59-60; CL3, L23-29); comprising:

for each transistor of the integrated circuit having a first threshold voltage level, calculating a first value based at least in part on delay and leakage corresponding to a second threshold voltage level (CL2, L1-2; CL3, L7-21; CL1, L30-33; CL5, L47-54);

selecting one of the transistors of the integrated circuit based on the first values (CL3, L25-29; CL5, L14-26); and

setting the selected one of the transistors to the second threshold voltage level (CL3, L25-29).

RE does not expressly teach modifying an area of at least one transistor within the integrated circuit. **PU** teaches modifying an area of at least one transistor within the integrated circuit (Fig. 3, BLK 315; CL2, L23-25; CL2, L47-50; CL2, L55-56), as increasing the area of transistors in the design will decrease the time delay in signal transmission and increase the size and power consumption (CL2, L23-25) and decreasing the area will have the opposite effects. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **RE** with the method of **PU** that included modifying an area of at least one transistor within the integrated circuit, as increasing the area of transistors in the design would decrease the time delay in signal transmission and increase the size and power consumption and decreasing the area would have the opposite effects.

Dependent claims

Per Claim 25: **RE** and **PU** teach the method of Claim 21. **RE** does not expressly teach sizing the integrated circuit to a predetermined area after modifying the area of the at least one transistor. **PU** teaches sizing the integrated circuit to a predetermined area after modifying the

area of the at least one transistor (Abstract L1-15; CL1, L65 to CL2, L1; CL2, L12-17; CL2, L55-56), as one of the criteria in designing the integrated circuit is that it requires smallest amount of area to implement (CL2, L15-17); and increasing the area of transistors in the design will decrease the time delay in signal transmission and increase the size and power consumption (CL2, L23-25) and decreasing the area will have the opposite effects. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **RE** with the method of **PU** that included sizing the integrated circuit to a predetermined area after modifying the area of the at least one transistor, as one of the criteria in designing the integrated circuit would be that it required smallest amount of area to implement and increasing the area of transistors in the design would decrease the time delay in signal transmission and increase the size and power consumption and decreasing the area would have the opposite effects.

Per Claim 27: **RE** and **PU** teach the method of Claim 25. **RE** does not expressly teach that the integrated circuit has a first area prior to calculating the first values and the predetermined area approximately equals the first area. **PU** teaches that the integrated circuit has a first area prior to calculating the first values and the predetermined area approximately equals the first area (Abstract L1-15; CL1, L65 to CL2, L1; CL2, L12-17; CL2, L55-56), as one of the criteria in designing the integrated circuit is that it requires smallest amount of area to implement (CL2, L15-17); and increasing the area of transistors in the design will decrease the time delay in signal transmission and increase the size and power consumption (CL2, L23-25) and decreasing the area will have the opposite effects. It would have been obvious to one of ordinary skill in the

art at the time of Applicants' invention to modify the method of **RE** with the method of **PU** that included the integrated circuit having a first area prior to calculating the first values and the predetermined area approximately equaled the first area, as one of the criteria in designing the integrated circuit would be that it required smallest amount of area to implement and increasing the area of transistors in the design would decrease the time delay in signal transmission and increase the size and power consumption and decreasing the area would have the opposite effects.

Per Claim 28: **RE** and **PU** teach the method of Claim 25. **RE** teaches determining a circuit performance (Fig. 2, Step 46); and

if the circuit performance is below a predetermined performance level, repeating calculating the first values, selecting one of the transistors, setting the selected one of the transistors (CL3, L39-45).

RE does not expressly teach modifying the area of the at least one transistor, and sizing the integrated circuit. **PU** teaches modifying the area of the at least one transistor, and sizing the integrated circuit (Fig. 3, BLK 315; CL2, L23-25; CL2, L47-50; CL2, L55-56), as one of the criteria in designing the integrated circuit is that it requires smallest amount of area to implement (CL2, L15-17); and increasing the area of transistors in the design will decrease the time delay in signal transmission and increase the size and power consumption (CL2, L23-25) and decreasing the area will have the opposite effects. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **RE** with the method of **PU** that included modifying the area of the at least one transistor, and sizing the integrated circuit, as one

of the criteria in designing the integrated circuit would be that it required smallest amount of area to implement and increasing the area of transistors in the design would decrease the time delay in signal transmission and increase the size and power consumption and decreasing the area would have the opposite effects.

Per Claim 29: **RE** and **PU** teach the method of Claim 21. **RE** teaches determining a circuit performance (Fig. 2, Step 46); and

if the circuit performance is below a predetermined performance level, repeating calculating the first values, selecting one of the transistors, setting the selected one of the transistors (CL3, L39-45).

RE does not expressly teach modifying the area of the at least one transistor, and sizing the integrated circuit. **PU** teaches modifying the area of the at least one transistor, and sizing the integrated circuit (Fig. 3, BLK 315; CL2, L23-25; CL2, L47-50; CL2, L55-56), as one of the criteria in designing the integrated circuit is that it requires smallest amount of area to implement (CL2, L15-17); and increasing the area of transistors in the design will decrease the time delay in signal transmission and increase the size and power consumption (CL2, L23-25) and decreasing the area will have the opposite effects. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **RE** with the method of **PU** that included modifying the area of the at least one transistor, and sizing the integrated circuit, as one of the criteria in designing the integrated circuit would be that it required smallest amount of area to implement and increasing the area of transistors in the design would decrease the time delay in

signal transmission and increase the size and power consumption and decreasing the area would have the opposite effects.

10.2 As per Claim 31, **RE** and **PU** teach the method of Claim 21. **RE** teaches an improved integrated circuit manufactured using the method of claim 21 (Fig. 1; Fig. 2).

11. Claims 22-24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Reyes et al. (RE)** (U.S. Patent 5,774,367) in view of **Pullela et al. (PU)** U.S. Patent 5,751,593), and further in view of **Gristede et al. (GR)** (U.S. Patent 6,175,949).

11.1 As per Claim 22, **RE** and **PU** teach the method of Claim 21. **RE** and **PU** do not expressly teach determining a cone of influence of the selected one of the transistors wherein the at least one transistor is within the cone of influence. **GR** teaches determining a cone of influence of the selected one of the transistors wherein the at least one transistor is within the cone of influence (CL1, L59-65), as cone of influence includes all objects driving a node or being driven by a node in the working schematic (CL5, L14-16) and the cone of influence permits faster and more efficient sizing of paths in the circuit (CL6, L32-38). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **RE** and **PU** with the method of **GR** that included determining a cone of influence of the selected one of the transistors wherein the at least one transistor was within the cone of influence, as cone of influence would include all objects driving a node or being driven by a

node in the working schematic and the cone of influence would permit faster and more efficient sizing of paths in the circuit.

Per Claim 23: **RE, PU** and **GR** teach the method of Claim 22. **RE** and **GR** do not expressly teach that the selected one of the transistors and the at least one transistor is a same transistor. **PU** teaches that the selected one of the transistors and the at least one transistor is a same transistor (Fig. 3, BLK 315; CL2, L23-25; CL2, L47-50; CL2, L55-56), as increasing the area of the transistor in the design will decrease the time delay in signal transmission and increase the size and power consumption (CL2, L23-25) and decreasing the area will have the opposite effects. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **RE** and **GR** with the method of **PU** that included the selected one of the transistors and the at least one transistor being the same transistor, as increasing the area of the transistor in the design would decrease the time delay in signal transmission and increase the size and power consumption and decreasing the area would have the opposite effects.

Per Claim 24: **RE, PU** and **GR** teach the method of Claim 22. **RE** and **GR** do not expressly teach that modifying includes modifying an area of each transistor within the cone of influence. **PU** teaches that modifying includes modifying an area of each transistor within the cone of influence (Fig. 3, BLK 315; CL2, L23-25; CL2, L47-50; CL2, L55-56), as increasing the area of the transistors in the design will decrease the time delay in signal transmission and increase the size and power consumption (CL2, L23-25) and decreasing the area will have the

opposite effects. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **RE** and **GR** with the method of **PU** that included modifying including modifying an area of each transistor within the cone of influence, as increasing the area of the transistors in the design would decrease the time delay in signal transmission and increase the size and power consumption and decreasing the area would have the opposite effects.

Per Claim 26: **RE** and **PU** teach the method of Claim 21. **RE** and **PU** do not expressly teach determining a cone of influence of the selected one of the transistors. **GR** teaches determining a cone of influence of the selected one of the transistors (CL1, L59-65), as cone of influence includes all objects driving a node or being driven by a node in the working schematic (CL5, L14-16) and the cone of influence permits faster and more efficient sizing of paths in the circuit (CL6, L32-38). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **RE** and **PU** with the method of **GR** that included determining a cone of influence of the selected one of the transistors, as cone of influence would include all objects driving a node or being driven by a node in the working schematic and the cone of influence would permit faster and more efficient sizing of paths in the circuit.

RE and **GR** do not expressly teach that modifying includes modifying an area of each transistor within the cone of influence. **PU** teaches that modifying includes modifying an area of each transistor within the cone of influence (Fig. 3, BLK 315; CL2, L23-25; CL2, L47-50; CL2, L55-56), as increasing the area of the transistors in the design will decrease the time delay in

signal transmission and increase the size and power consumption (CL2, L23-25) and decreasing the area will have the opposite effects. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **RE** and **GR** with the method of **PU** that included modifying including modifying an area of each transistor within the cone of influence, as increasing the area of the transistors in the design would decrease the time delay in signal transmission and increase the size and power consumption and decreasing the area would have the opposite effects.

12. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Reyes et al. (RE)** (U.S. Patent 5,774,367) in view of **Gristede et al. (GR)** (U.S. Patent 6,175,949).

12.1 As per Claim 43, **RE** teaches a computer readable medium for analyzing an integrated circuit having a plurality of transistors (Fig. 2; CL2, L59-60; CL3, L23-29);

each of the plurality of transistors having a first threshold voltage level (CL2, L1-2); comprising:

a first plurality of instructions for calculating a first value based at least in part on delay and leakage corresponding to a second voltage level for each of the plurality of transistors (CL2, L1-2; CL3, L7-21; CL1, L30-33; CL5, L47-54);

a second plurality of instructions for selecting one of the plurality of transistors based on the first values (CL3, L25-29; CL5, L14-26); and

a third plurality of instructions for setting the selected one of the transistors to the second threshold voltage (CL3, L25-29).

RE does not expressly teach a fourth plurality of instructions for determining a cone of influence of the selected one of the transistors. **GR** teaches a fourth plurality of instructions for determining a cone of influence of the selected one of the transistors e (CL1, L59-65), as cone of influence includes all objects driving a node or being driven by a node in the working schematic (CL5, L14-16) and the cone of influence permits faster and more efficient sizing of paths in the circuit (CL6, L32-38). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer readable medium of **RE** with the computer readable medium of **GR** that included a fourth plurality of instructions for determining a cone of influence of the selected one of the transistors, as cone of influence would include all objects driving a node or being driven by a node in the working schematic and the cone of influence would permit faster and more efficient sizing of paths in the circuit.

Allowable Subject Matter

13. Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claims 1-20, 32-38, 41, 42 and 44 are allowed.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to the Applicants' disclosure.

The following patents and papers are cited to further show the state of the art at the time of Applicants' invention with respect to method and system for selecting device threshold voltages for improving performance and minimizing leakage power loss.

1. Bertin et al, "ASIC low power activity detector to change threshold voltage", U.S. Patent 5,778,204, April 2000.
2. Sundararajan et al, "Low power synthesis of dual threshold voltage CMOS VLSI circuits", ACM, 1999.
3. De et al., "Circuit including forward body bias from supply voltage and ground nodes", U.S. Patent 6,300,819, October 2001.
4. Mizuno et al., "Semiconductor integrated circuit device and microcomputer", U.S. Patent 6,608,509, August 2003.
5. De et al., "Method and apparatus for reducing standby leakage current using a transistor stack effect", U.S. Patent 6,169,419, June 2001.
6. Bosshart, "Dynamic logic circuits using transistors having differing threshold voltages", U.S. Patent 5,831,451, November 1998.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7329.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
September 24, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER